



GP 2185

PATENT
2207/9865

THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT : Manoj KHARE et al.

SERIAL NO. : 09/749,660

COPY OF PAPERS
ORIGINALLY FILED

FILING DATE : 12/28/2000

GROUP ART UNIT : 2185

FOR : METHOD AND APPARATUS FOR REDUCING MEMORY
LATENCY IN A CACHE COHERENT MULTI-NODE
ARCHITECTURE

EXAMINER : Unknown

Commissioner of Patents
Washington, D.C. 20231RECEIVED
MAY 08 2002
Technology Center 2100INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97

S I R:

In accordance with Applicant's duty of disclosure under 37 C.F.R. §1.56(a) and §1.97(c), the references listed on the attached form PTO-1449 are hereby brought to the Examiner's attention. Copies of the first page of each reference only is enclosed. Also enclosed is a Compact disc (CD) containing a complete set of all the references listed. Hard copies of the references listed can be provided should the Examiner prefer to do so. These references were uncovered through a keyword computer search. Based on the titles for these patent references, they are considered less relevant than the IDS filed on February 25, 2002.

It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear in the "references cited" on any patent to issue therefrom.

Respectfully submitted,

KENYON & KENYON

Date: April 14, 2002

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CERTIFICATE OF MAILING

I hereby certify that the following documents are being deposited with the United States Postal Service as First Class Mail in a large envelope addressed to: Commissioner for Patents, Washington, DC 20231, with regard to Docket No. 2207/9865, Serial No. 09/749,660

1. Information Disclosure Statement Under 37 C.F.R. 1.97
2. 1st page only for 58 References Listed on IDS
3. 1 CD containing complete set of all 58 References
4. Postcard

Dated: April 18, 2002

KENYON & KENYON

By: Pilar Rodriguez
Pilar M. Rodriguez

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